Application Note 122
Using Dallas' 1-Wire® Chips in 1-cell Li+ battery packs with low-side n-channel safety FETs

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OVERVIEW

Dallas' 1-Wire battery management products are designed with the strategy to minimize electronics in the battery pack while utilizing host-system resources whenever possible, to minimize battery pack cost. The hardware design of a Dallas-based battery pack is quite simple, with very few external components required. This application note addresses the implementation of a Dallas-based Li-Ion (Li^+) battery pack with low-side n-channel safety FETs. A reference design using DS182x 1-Wire digital thermometer is presented focusing on Li^+ cell safety and ESD-hardness.

Li^+ SAFETY CONSIDERATIONS

Safety will be considered first. Dallas recommends that no circuit should exist on the Li^+ cell side of the safety FETs. Such a connection could compromise overall safety of the battery pack by potentially bypassing the safety FETs. An example of such a case is illustrated in Figure 1.

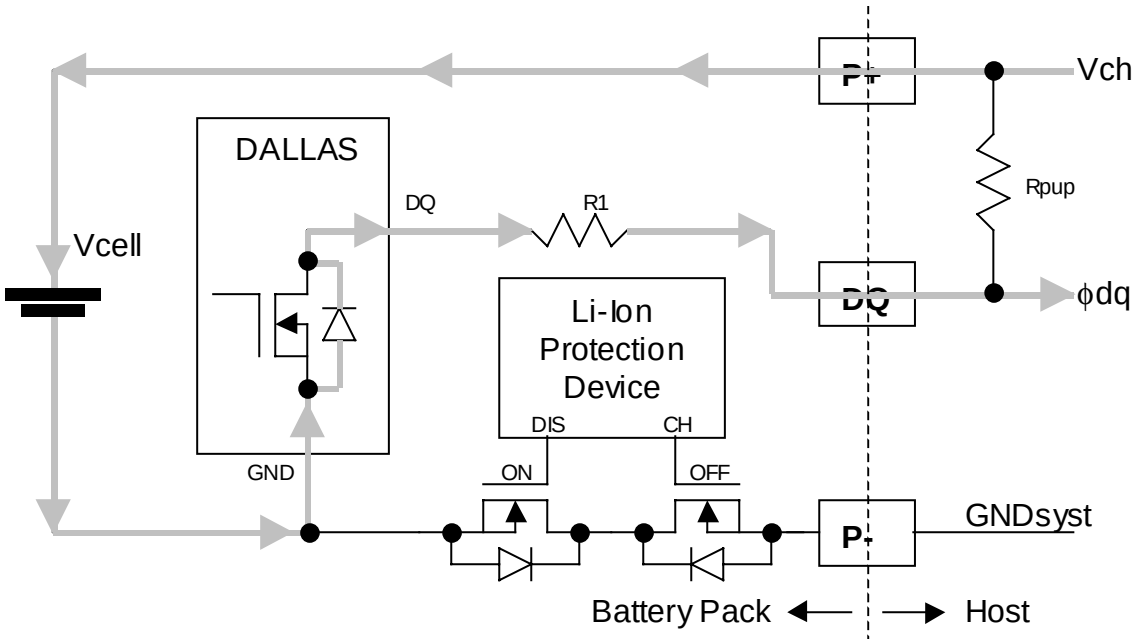

Figure 1. **Potential charging path that bypasses safety FETs if Dallas chip is on the cell side of the FETs**

The drain-to-body diode of the n-channel open-drain DQ output driver of the Dallas chip could provide a charging path (highlighted in Figure 1) through the device that will bypass the protection FETs. This conduction path will exist only if the potential difference between V_{CH} and ϕ_{DQ} is more than a diode drop greater than the sum of V_{CELL} and the voltage drop across R1. While such a condition is unlikely, it does illustrate a possible way to bypass the safety circuit if the Dallas chip is connected on the cell side of the safety FETs. Dallas thus recommends connecting the Dallas battery management device on the terminal side of the safety FETs, unless otherwise recommended by the Li^+ cell manufacturer.

DALLAS REFERENCE DESIGN

Figure 2 below illustrates the recommended implementation of the Dallas DS18B20 (or DS1822) with respect to the low-side n-channel safety FETs. Additionally, Dallas recommends passive devices that primarily serve to protect the DS182x from ESD damage or a latchup state resulting from ESD. The protection offered by each device is described below:

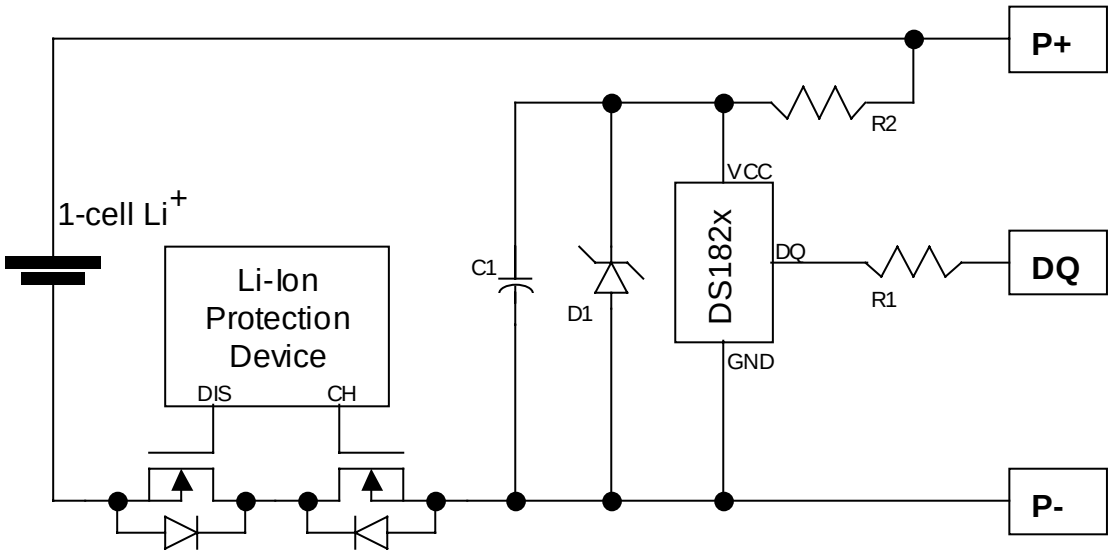

Figure 2. **Recommended schematic for single-cell Li^+ pack with low-side n-channel protection FETs**

1. The capacitor C1 on V_{CC} is simply a high-frequency bypass cap. 0.1 µF is recommended.
2. The 5.1 volt Zener D1 on V_{CC} serves two purposes. It clamps at the Zener voltage of 5.1 volt so that excessive DC voltage, ESD, and switching transients cannot damage the DS182x through V_{CC}. In the forward bias region , it clamps around 0.7 volt, thereby disallowing V_{CC} from falling more than 0.7 volt below GND, which is possible when both the CHarge and DIScharge FETs are high impedance.
3. The resistor R1 in series with DQ limits current through the large ESD protection diode internally connected between DQ and GND. R1 ≥ 470Ω is recommended, but consider the size of the pullup on DQ (which is generally installed in the host system) and the DQ I/O specs before setting this value.
4. The resistor R2 in series with V_{CC} limits current so that ESD-induced latchup cannot occur. R2 ≥ 120Ω is recommended, and should have very little effect on supply voltage at DS182x max spec current of 1.5 mA. In choosing R2, also consider the power dissipation via R2 and D1 if your application allows Pack+ (P+) voltage to reach well above the Zener clamp voltage.

In summary, very few components are required in a Dallas-based Li^+ battery pack. This application note considered the common implementation of low side n-channel safety FETs. Dallas recommends that the Dallas device be connected on the terminal side of the safety FETs so that no potential charging paths exist that bypass the FETs. A reference design is recommended for the DS182x 1-Wire digital thermometer, including 4 passive components that increase the ESD-hardness of the battery pack beyond ±15 kV per the IEC1000-4-2 model.