Application Note 501
Interfacing 3-wire Real Time Clocks With A Microcontroller

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Dallas Semiconductor offers a variety of serial Real Time Clocks (RTCs). A number of these use a 3-wire interface to communicat with a microprocessor.

This application note is intended to help customers understand the basics of the 3-wire interface.

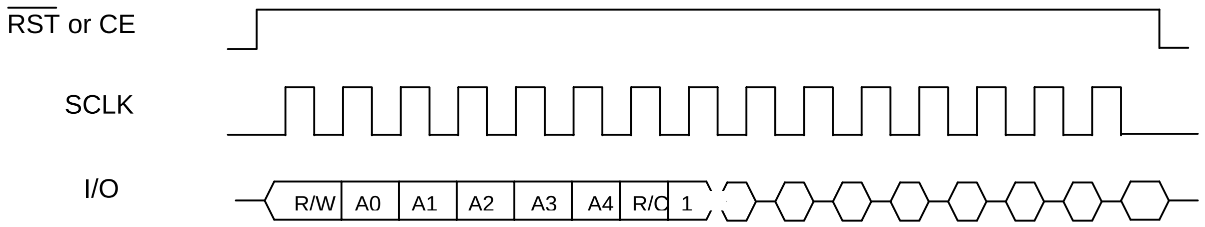
OVERVIEW

Figure 1 shows a typical single byte read and single byte write for the DS1302. Other 3-wire parts may have a different command byte structure. However, the timing sequence remains the same. Note that data are clocked into the RTC on the rising edge of SCLK. The RTC outputs data on the falling edge of SCLK. On some clocks, data will remain valid until the next falling edge of SCLK. On most of the newer 3-wire clocks, however, the output will go high Z on the rising edge of SCLK. To help insure possible upgrade compatibility, it is usually best to read data from the RTC before the rising edge of SCLK occurs (but after the Clock to Data Delay).

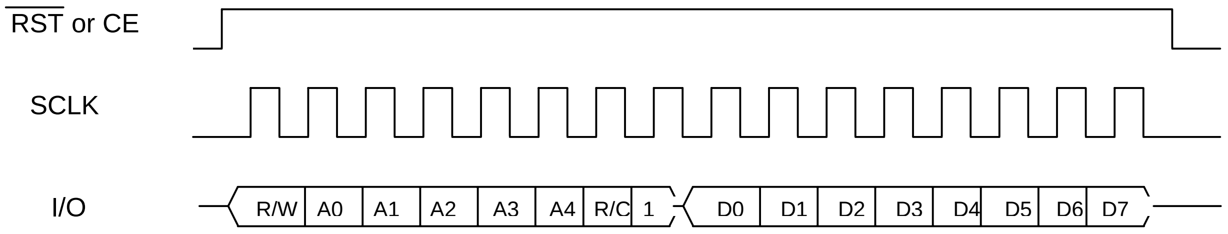
Note that during a read, the clock goes from reading the command byte to outputting data on one SCLK cycle. The processor must release the data line after the rising clock edge (after Tcdh). The RTC takes control of the data line on the falling edge of the clock.

DATA TRANSFER SUMMARY Figure 1

Single Byte Read



Single Byte Write



In burst mode, $\overline{\text{RST}}$ is kept high and additional SCLK cycles are sent until the end of the burst.

At the beginning of a data transfer, SCLK should be low. If SCLK is high when $\overline{\text{RST}}$/CE is brought active, the RTC may interpret that as a low to high transition of SCLK.

An example of 3-wire code, written for the DS1302, is available at:
ftp://ftp.dalsemi.com/pub/timekeeping/Ex_1302C.txt

SUMMARY

Following the information above will help insure that 3-wire communication routines will function correctly.